

# NTMFS4C09N

## Power MOSFET

30 V, 52 A, Single N-Channel, SO-8 FL

### Features

- Low  $R_{DS(on)}$  to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### Applications

- CPU Power Delivery
- DC-DC Converters

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter	Symbol	Value	Unit	
Drain-to-Source Voltage	$V_{DS}$	30	V	
Gate-to-Source Voltage	$V_{GS}$	$\pm 20$	V	
Continuous Drain Current $R_{\theta JA}$ (Note 1)	$I_D$	$T_A = 25^\circ\text{C}$	16.4	A
		$T_A = 80^\circ\text{C}$	12.3	
Power Dissipation $R_{\theta JA}$ (Note 1)	$P_D$	$T_A = 25^\circ\text{C}$	2.51	W
		$T_A = 80^\circ\text{C}$		
Continuous Drain Current $R_{\theta JA} \leq 10$ s (Note 1)	$I_D$	$T_A = 25^\circ\text{C}$	25.3	A
		$T_A = 80^\circ\text{C}$	19.0	
Power Dissipation $R_{\theta JA} \leq 10$ s (Note 1)	$P_D$	$T_A = 25^\circ\text{C}$	6.0	W
		$T_A = 80^\circ\text{C}$		
Continuous Drain Current $R_{\theta JA}$ (Note 2)	$I_D$	$T_A = 25^\circ\text{C}$	9.0	A
		$T_A = 80^\circ\text{C}$	6.8	
Power Dissipation $R_{\theta JA}$ (Note 2)	$P_D$	$T_A = 25^\circ\text{C}$	0.76	W
		$T_A = 80^\circ\text{C}$		
Continuous Drain Current $R_{\theta JC}$ (Note 1)	$I_D$	$T_C = 25^\circ\text{C}$	52	A
		$T_C = 80^\circ\text{C}$	39	
Power Dissipation $R_{\theta JC}$ (Note 1)	$P_D$	$T_C = 25^\circ\text{C}$	25.5	W
		$T_C = 80^\circ\text{C}$		
Pulsed Drain Current	$T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$	$I_{DM}$	146	A
Current Limited by Package	$T_A = 25^\circ\text{C}$	$I_{Dmax}$	80	A
Operating Junction and Storage Temperature	$T_J, T_{STG}$		-55 to +150	$^\circ\text{C}$
Source Current (Body Diode)		$I_S$	23	A
Drain to Source $dV/dt$		$dV/dt$	7.0	V/ns
Single Pulse Drain-to-Source Avalanche Energy ( $T_J = 25^\circ\text{C}, V_{GS} = 10$ V, $I_L = 29$ A <sub>pk</sub> , $L = 0.1$ mH, $R_{GS} = 25 \Omega$ ) (Note 3)		$E_{AS}$	42	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		$T_L$	260	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

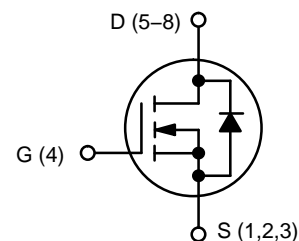
1. Surface-mounted on FR4 board using 1 sq-in pad, 1 oz Cu.
2. Surface-mounted on FR4 board using the minimum recommended pad size.
3. Parts are 100% tested at  $T_J = 25^\circ\text{C}, V_{GS} = 10$  V,  $I_L = 20$  A<sub>pk</sub>,  $E_{AS} = 20$  mJ.



ON Semiconductor®

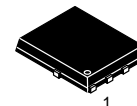
[www.onsemi.com](http://www.onsemi.com)

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	$I_D$ MAX
30 V	5.8 m $\Omega$ @ 10 V	52 A
	8.5 m $\Omega$ @ 4.5 V	

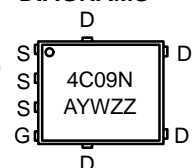


N-CHANNEL MOSFET

### MARKING DIAGRAMS



SO-8 FLAT LEAD  
CASE 488AA  
STYLE 1



- A = Assembly Location
- Y = Year
- W = Work Week
- ZZ = Lot Traceability

### ORDERING INFORMATION

Device	Package	Shipping†
NTMFS4C09NT1G	SO-8 FL (Pb-Free)	1500 / Tape & Reel
NTMFS4C09NT3G	SO-8 FL (Pb-Free)	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NTMFS4C09N

## THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case (Drain)	$R_{\theta JC}$	4.9	°C/W
Junction-to-Ambient – Steady State (Note 4)	$R_{\theta JA}$	49.8	
Junction-to-Ambient – Steady State (Note 5)	$R_{\theta JA}$	164.6	
Junction-to-Ambient – ( $t \leq 10$ s) (Note 4)	$R_{\theta JA}$	21.0	

- Surface-mounted on FR4 board using 1 sq-in pad, 1 oz Cu.
- Surface-mounted on FR4 board using the minimum recommended pad size.

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
-----------	--------	----------------	-----	-----	-----	------

### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	30			V
Drain-to-Source Breakdown Voltage (transient)	$V_{(BR)DSS(t)}$	$V_{GS} = 0\text{ V}, I_{D(aval)} = 8.4\text{ A}, T_{case} = 25^\circ\text{C}, t_{transient} = 100\text{ ns}$	34			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			14.4		mV/°C
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0\text{ V}, V_{DS} = 24\text{ V}$			1.0	$\mu\text{A}$
		$T_J = 25^\circ\text{C}$			10	
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA

### ON CHARACTERISTICS (Note 6)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	1.3		2.1	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			4.8		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 30\text{ A}$		4.6	5.8	m $\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 18\text{ A}$		6.8	8.5	
Forward Transconductance	$g_{FS}$	$V_{DS} = 1.5\text{ V}, I_D = 15\text{ A}$		50		S
Gate Resistance	$R_G$	$T_A = 25^\circ\text{C}$	0.3	1.0	2.0	$\Omega$

### CHARGES AND CAPACITANCES

Input Capacitance	$C_{ISS}$	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 15\text{ V}$		1252		pF
Output Capacitance	$C_{OSS}$			610		
Reverse Transfer Capacitance	$C_{RSS}$			126		
Capacitance Ratio	$C_{RSS}/C_{ISS}$	$V_{GS} = 0\text{ V}, V_{DS} = 15\text{ V}, f = 1\text{ MHz}$		0.101		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}; I_D = 30\text{ A}$		10.9		nC
Threshold Gate Charge	$Q_{G(TH)}$			1.9		
Gate-to-Source Charge	$Q_{GS}$			3.4		
Gate-to-Drain Charge	$Q_{GD}$			5.4		
Gate Plateau Voltage	$V_{GP}$			3.1		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 15\text{ V}; I_D = 30\text{ A}$		22.2		nC

### SWITCHING CHARACTERISTICS (Note 7)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}, I_D = 15\text{ A}, R_G = 3.0\ \Omega$		10		ns
Rise Time	$t_r$			32		
Turn-Off Delay Time	$t_{d(OFF)}$			16		
Fall Time	$t_f$			6.0		

- Pulse Test: pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$ .
- Switching characteristics are independent of operating junction temperatures.

# NTMFS4C09N

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>SWITCHING CHARACTERISTICS</b> (Note 7)						
Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 10\text{ V}, V_{DS} = 15\text{ V},$ $I_D = 15\text{ A}, R_G = 3.0\ \Omega$		7.0		ns
Rise Time	$t_r$			28		
Turn-Off Delay Time	$t_{d(OFF)}$			20		
Fall Time	$t_f$			4.0		

## DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	$V_{SD}$	$V_{GS} = 0\text{ V},$ $I_S = 10\text{ A}$	$T_J = 25^\circ\text{C}$		0.79	1.1	V
			$T_J = 125^\circ\text{C}$		0.65		
Reverse Recovery Time	$t_{RR}$	$V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s},$ $I_S = 30\text{ A}$		31		ns	
Charge Time	$t_a$			15			
Discharge Time	$t_b$			16			
Reverse Recovery Charge	$Q_{RR}$			15		nC	

6. Pulse Test: pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$ .

7. Switching characteristics are independent of operating junction temperatures.

# NTMFS4C09N

## TYPICAL CHARACTERISTICS

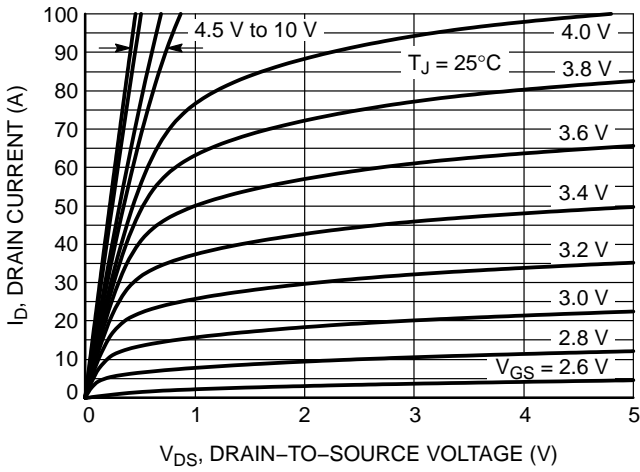


Figure 1. On-Region Characteristics

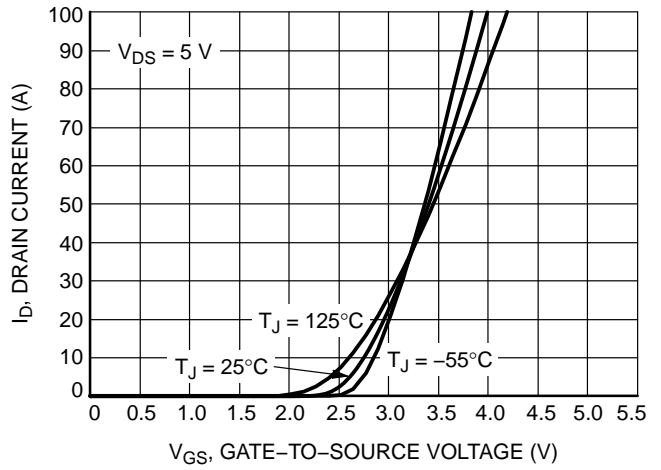


Figure 2. Transfer Characteristics

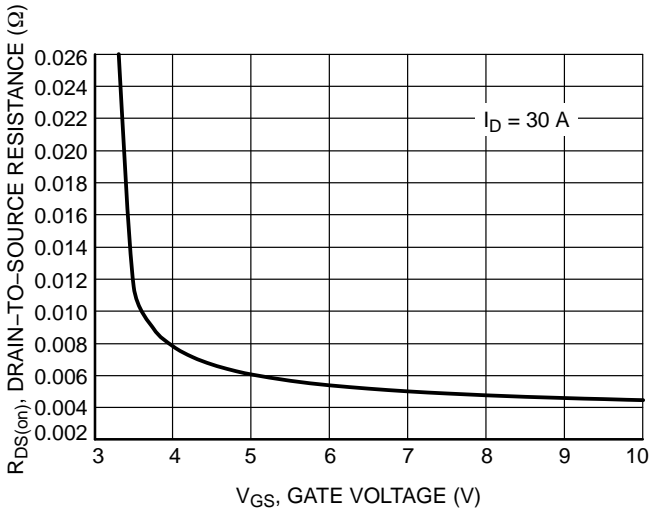


Figure 3. On-Resistance vs. Gate-to-Source Voltage

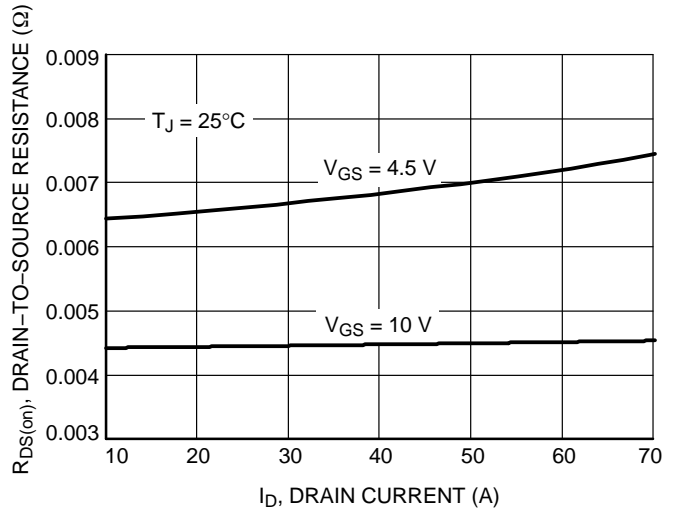


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

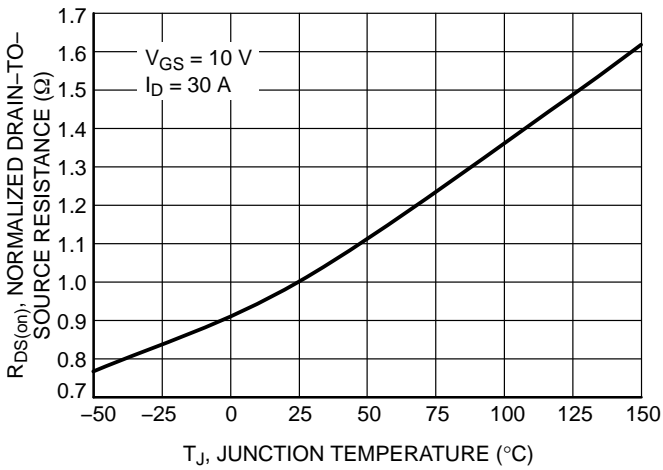


Figure 5. On-Resistance Variation with Temperature

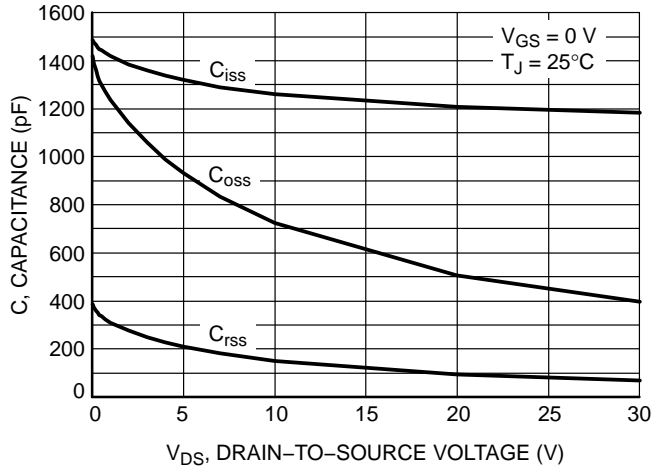
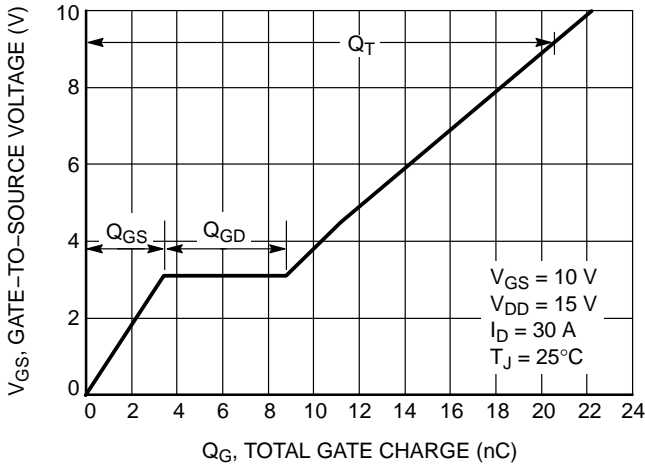


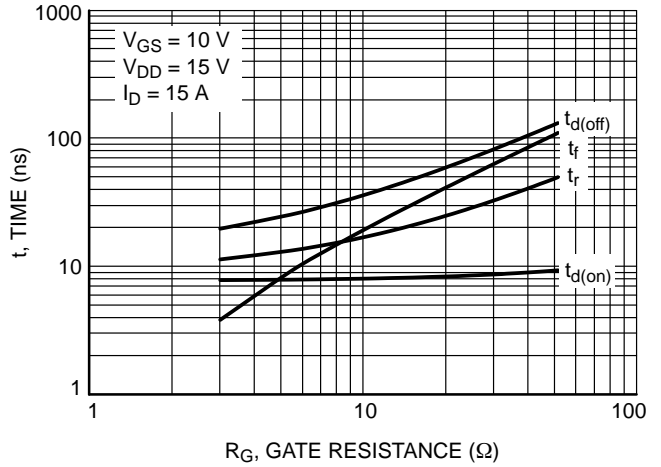
Figure 6. Capacitance Variation

# NTMFS4C09N

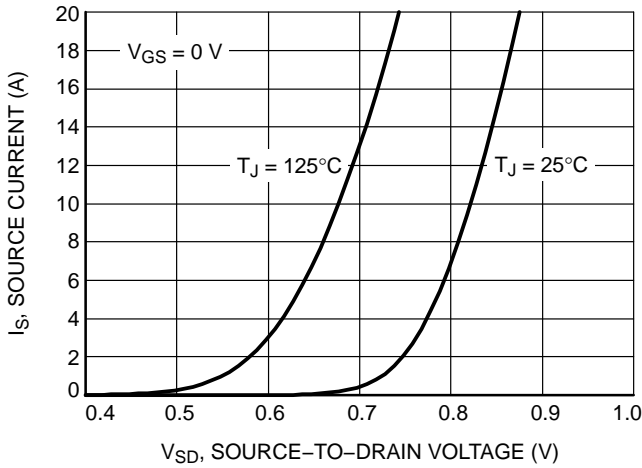
## TYPICAL CHARACTERISTICS



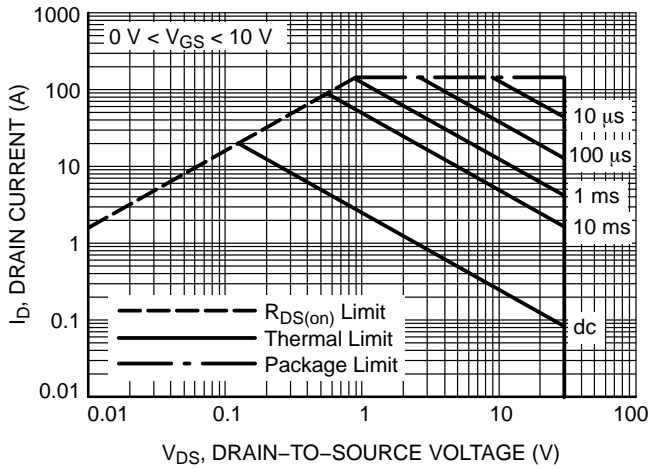
**Figure 7. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge**



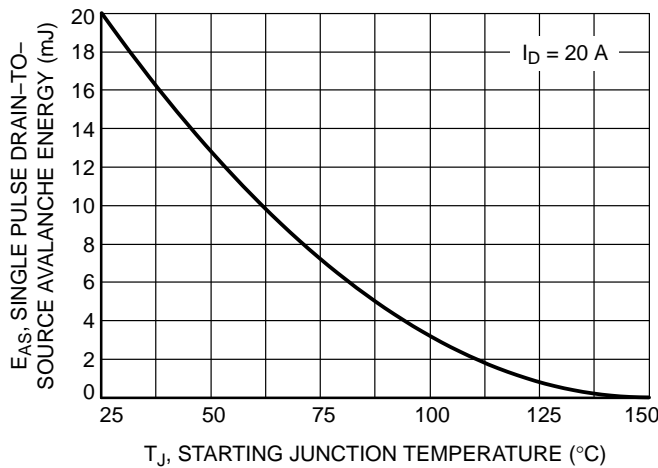
**Figure 8. Resistive Switching Time Variation vs. Gate Resistance**



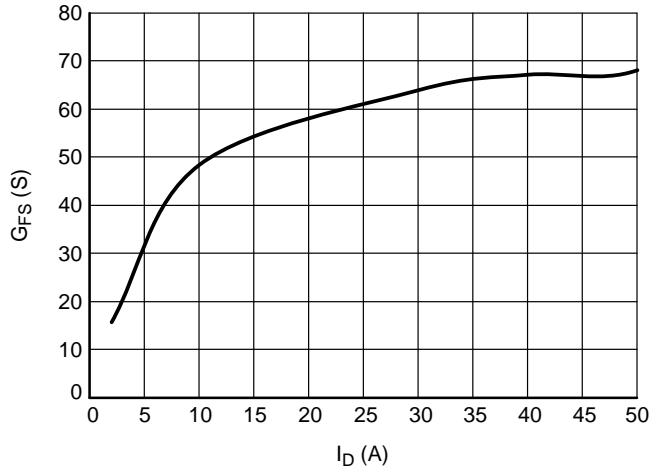
**Figure 9. Diode Forward Voltage vs. Current**



**Figure 10. Maximum Rated Forward Biased Safe Operating Area**



**Figure 11. Maximum Avalanche Energy vs. Starting Junction Temperature**



**Figure 12.  $G_{FS}$  vs.  $I_D$**

# NTMFS4C09N

## TYPICAL CHARACTERISTICS

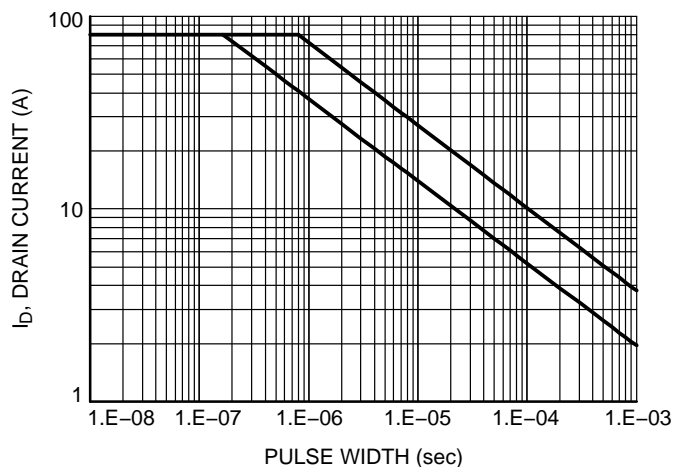


Figure 13. Avalanche Characteristics

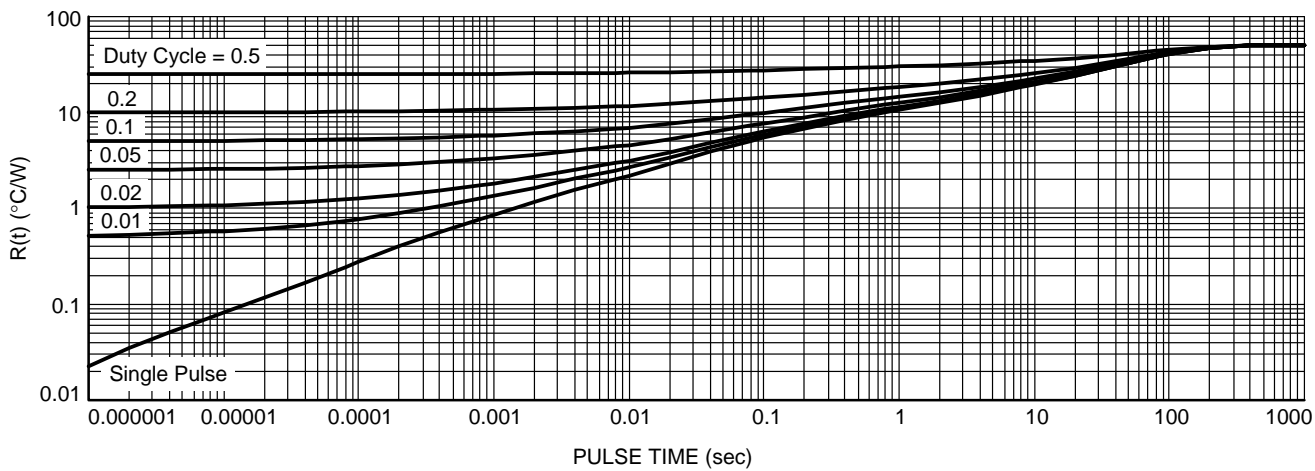
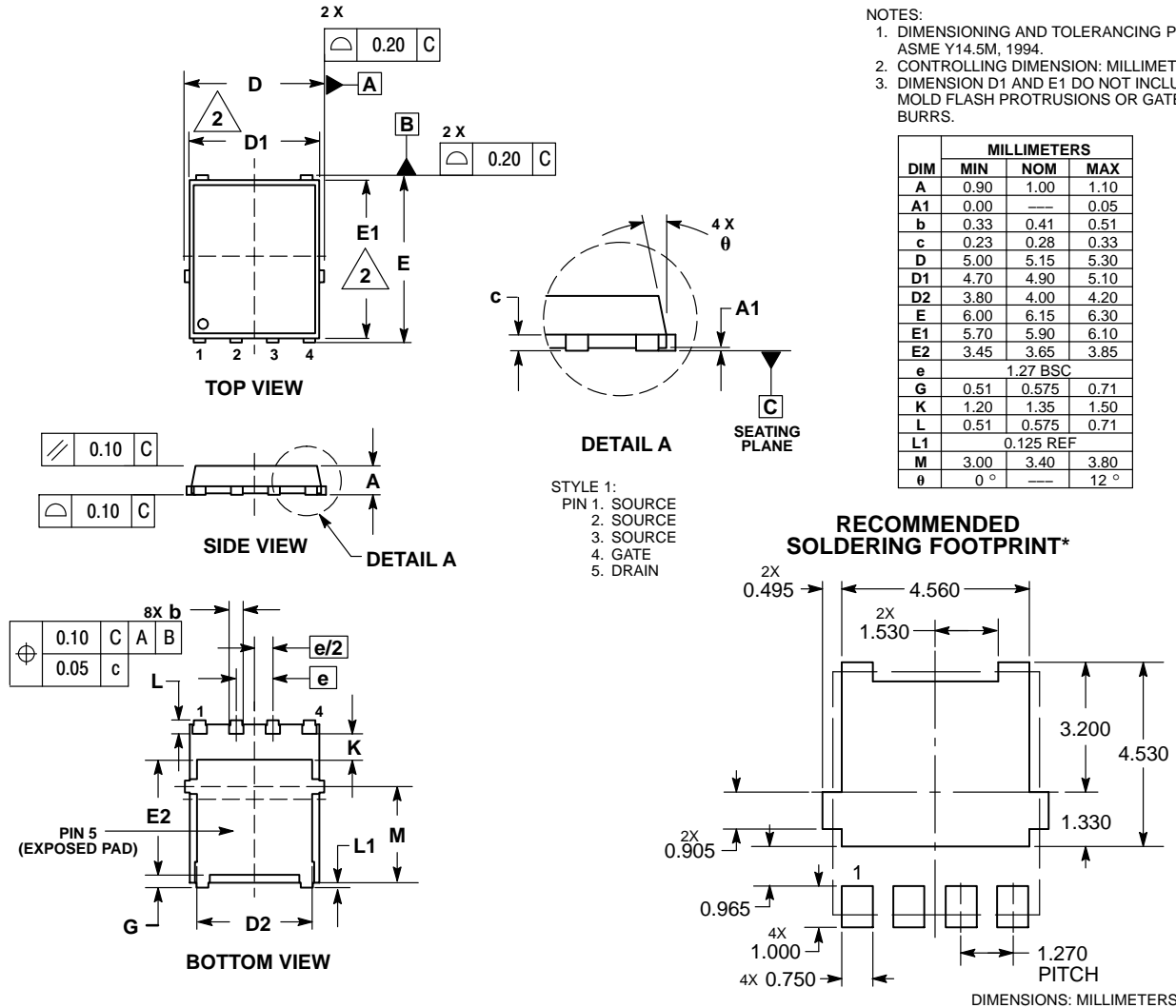


Figure 14. Thermal Response

# NTMFS4C09N

## PACKAGE DIMENSIONS

DFN5 5x6, 1.27P  
(SO-8FL)  
CASE 488AA  
ISSUE M



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and the are registered trademarks of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries. SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marketing.pdf](http://www.onsemi.com/site/pdf/Patent-Marketing.pdf). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

### PUBLICATION ORDERING INFORMATION

#### LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
Email: [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**N. American Technical Support:** 800-282-9855 Toll Free USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
Phone: 81-3-5817-1050

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)

**Order Literature:** <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative